l -	vnamic onfig	Minor Error Bits The bits of this word are set by the processor to indicate that a minor error has occurred in your ladder program. Minor errors, bits 0 to 7, revert to major error 0020H if any bit is detected as being set at the end of the scan. HHT users: If the processor faults for error code 0020H, you must clear minor error bits S:5/0–7 along with S:1/13 to attempt error recovery. Overflow Trap Bit	•	•	•	•	•
		When this bit is set by the processor, it indicates that a mathematical overflow has occurred in the ladder program. See S:0/1 for more information. If this bit is ever set upon execution of the END, TND, or REF instruction, major error (0020) will be declared. To avoid this type of major error from occurring, examine the state of this bit following a math instruction (ADD, SUB, MUL, DIV, DDV, NEG, SCL, TOD, or FRD), take appropriate action, and then clear bit S:5/0 using an OTU instruction with S:5/0 or a CLR instruction with S:5.	•	•	•	•	•
S:5/1 N/A	′A	Reserved	•	•	•	•	•
Con	namic onfig	Control Register Error Bit The LFU, LFL, FFU, FFL, BSL, BSR, SQO, SQC, and SQL instructions are capable of generating this error. When bit S:5/2 is set, it indicates that the error bit of the control instruction has been set. If this bit is ever set upon execution of the END, TND, or REF instruction, major error (0020) will be declared. To avoid this type of major error from occurring, examine the state of this bit following a control register instruction, take appropriate action, and then clear bit S:5/2 using an OTU instruction with S:5/2 or a CLR instruction with S:5.	•	•	•	•	•
	rnamic onfig	Major Error Detected while Executing User Fault Routine Bit When set, the major error code (S:6) represents the major error that occurred while processing the fault routine due to another major error.		•	•	•	•

		state of this bit inside your fault routine, take appropriate action, and then clear bit					
		S:5/3 using an OTU instruction with S:5/3 or a CLR instruction with S:5.					
		Application example:					
		Suppose you are executing your					
		fault routine for a fault code 0016H					
		Startup Protection. At rung 3 inside					
		this fault routine, a TON containing a					
		negative preset is executed. When					
		rung 4 is executed, fault code 0016H					
		is overwritten to indicated code 0034H,					
		and S:5/3 is set. If your fault routine did not					
		determine that S:5/3 was set, major error					
		0020H would be declared at the end of the					
		first scan. To avoid this problem, examine					
		S:5/3, followed by S:6, prior to returning					
		from your fault routine. If S:5/3 is set, take appropriate action to remedy the fault,					
		then clear S:5/3.					
S:5/4	Dynamic	M0-M1 Referenced on Disabled Slot					
3.5/4	Config	Bit This bit is set whenever any instruction					
		references an M0 or M1 module file					
		element for a slot that is disabled (via its I/O slot enable bit). When set, the bit					
		element for a slot that is disabled (via its					
		element for a slot that is disabled (via its I/O slot enable bit). When set, the bit					
		element for a slot that is disabled (via its I/O slot enable bit). When set, the bit indicates that an instruction could not					
		element for a slot that is disabled (via its I/O slot enable bit). When set, the bit indicates that an instruction could not execute properly due to the unavailability of the addressed or M0 or M1 data. If this bit is ever set upon execution		•	•	•	•
		element for a slot that is disabled (via its I/O slot enable bit). When set, the bit indicates that an instruction could not execute properly due to the unavailability of the addressed or M0 or M1 data. If this bit is ever set upon execution of the END, TND, or REF instruction,		•	•	•	•
		element for a slot that is disabled (via its I/O slot enable bit). When set, the bit indicates that an instruction could not execute properly due to the unavailability of the addressed or M0 or M1 data. If this bit is ever set upon execution of the END, TND, or REF instruction, major error (0020) is declared. To avoid this		•	•	•	•
		element for a slot that is disabled (via its I/O slot enable bit). When set, the bit indicates that an instruction could not execute properly due to the unavailability of the addressed or M0 or M1 data. If this bit is ever set upon execution of the END, TND, or REF instruction, major error (0020) is declared. To avoid this type of major error from occurring,		•	•	•	•
		element for a slot that is disabled (via its I/O slot enable bit). When set, the bit indicates that an instruction could not execute properly due to the unavailability of the addressed or M0 or M1 data. If this bit is ever set upon execution of the END, TND, or REF instruction, major error (0020) is declared. To avoid this type of major error from occurring, examine the state of this bit following a		•	•	•	•
		element for a slot that is disabled (via its I/O slot enable bit). When set, the bit indicates that an instruction could not execute properly due to the unavailability of the addressed or M0 or M1 data. If this bit is ever set upon execution of the END, TND, or REF instruction, major error (0020) is declared. To avoid this type of major error from occurring, examine the state of this bit following a M0-M1 referenced instruction, take		•	•	•	•
		element for a slot that is disabled (via its I/O slot enable bit). When set, the bit indicates that an instruction could not execute properly due to the unavailability of the addressed or M0 or M1 data. If this bit is ever set upon execution of the END, TND, or REF instruction, major error (0020) is declared. To avoid this type of major error from occurring, examine the state of this bit following a M0-M1 referenced instruction, take appropriate action, and then clear bit S:5/4		•	•	•	•
		element for a slot that is disabled (via its I/O slot enable bit). When set, the bit indicates that an instruction could not execute properly due to the unavailability of the addressed or M0 or M1 data. If this bit is ever set upon execution of the END, TND, or REF instruction, major error (0020) is declared. To avoid this type of major error from occurring, examine the state of this bit following a M0-M1 referenced instruction, take appropriate action, and then clear bit S:5/4 using and OTU instruction with S:5/4 or a		•	•	•	•
S.E /F +0	N/A	element for a slot that is disabled (via its I/O slot enable bit). When set, the bit indicates that an instruction could not execute properly due to the unavailability of the addressed or M0 or M1 data. If this bit is ever set upon execution of the END, TND, or REF instruction, major error (0020) is declared. To avoid this type of major error from occurring, examine the state of this bit following a M0-M1 referenced instruction, take appropriate action, and then clear bit S:5/4 using and OTU instruction with S:5/4 or a CLR instruction with S:5.		•	•	•	•
S:5/5 to	N/A	element for a slot that is disabled (via its I/O slot enable bit). When set, the bit indicates that an instruction could not execute properly due to the unavailability of the addressed or M0 or M1 data. If this bit is ever set upon execution of the END, TND, or REF instruction, major error (0020) is declared. To avoid this type of major error from occurring, examine the state of this bit following a M0-M1 referenced instruction, take appropriate action, and then clear bit S:5/4 using and OTU instruction with S:5/4 or a CLR instruction with S:5.	•	•	•	•	•
S:5/7		element for a slot that is disabled (via its I/O slot enable bit). When set, the bit indicates that an instruction could not execute properly due to the unavailability of the addressed or M0 or M1 data. If this bit is ever set upon execution of the END, TND, or REF instruction, major error (0020) is declared. To avoid this type of major error from occurring, examine the state of this bit following a M0-M1 referenced instruction, take appropriate action, and then clear bit S:5/4 using and OTU instruction with S:5/4 or a CLR instruction with S:5. Reserved for minor errors that revert to major errors at the end of the scan.	•	•	•	•	•
-	N/A Status	element for a slot that is disabled (via its I/O slot enable bit). When set, the bit indicates that an instruction could not execute properly due to the unavailability of the addressed or M0 or M1 data. If this bit is ever set upon execution of the END, TND, or REF instruction, major error (0020) is declared. To avoid this type of major error from occurring, examine the state of this bit following a M0-M1 referenced instruction, take appropriate action, and then clear bit S:5/4 using and OTU instruction with S:5/4 or a CLR instruction with S:5. Reserved for minor errors that revert to major errors at the end of the scan. Memory Module Boot Bit	•	•	•	•	•
S:5/7		element for a slot that is disabled (via its I/O slot enable bit). When set, the bit indicates that an instruction could not execute properly due to the unavailability of the addressed or M0 or M1 data. If this bit is ever set upon execution of the END, TND, or REF instruction, major error (0020) is declared. To avoid this type of major error from occurring, examine the state of this bit following a M0-M1 referenced instruction, take appropriate action, and then clear bit S:5/4 using and OTU instruction with S:5/4 or a CLR instruction with S:5. Reserved for minor errors that revert to major errors at the end of the scan. Memory Module Boot Bit When this bit is set by the processor,	•	•	•	•	•
S:5/7		element for a slot that is disabled (via its I/O slot enable bit). When set, the bit indicates that an instruction could not execute properly due to the unavailability of the addressed or M0 or M1 data. If this bit is ever set upon execution of the END, TND, or REF instruction, major error (0020) is declared. To avoid this type of major error from occurring, examine the state of this bit following a M0-M1 referenced instruction, take appropriate action, and then clear bit S:5/4 using and OTU instruction with S:5/4 or a CLR instruction with S:5. Reserved for minor errors that revert to major errors at the end of the scan. Memory Module Boot Bit When this bit is set by the processor, it indicates that a memory module program	•	•	•	•	•
S:5/7		element for a slot that is disabled (via its I/O slot enable bit). When set, the bit indicates that an instruction could not execute properly due to the unavailability of the addressed or M0 or M1 data. If this bit is ever set upon execution of the END, TND, or REF instruction, major error (0020) is declared. To avoid this type of major error from occurring, examine the state of this bit following a M0-M1 referenced instruction, take appropriate action, and then clear bit S:5/4 using and OTU instruction with S:5/4 or a CLR instruction with S:5. Reserved for minor errors that revert to major errors at the end of the scan. Memory Module Boot Bit When this bit is set by the processor, it indicates that a memory module program has been transferred to the processor. This	•	•	•	•	•
S:5/7		element for a slot that is disabled (via its I/O slot enable bit). When set, the bit indicates that an instruction could not execute properly due to the unavailability of the addressed or M0 or M1 data. If this bit is ever set upon execution of the END, TND, or REF instruction, major error (0020) is declared. To avoid this type of major error from occurring, examine the state of this bit following a M0-M1 referenced instruction, take appropriate action, and then clear bit S:5/4 using and OTU instruction with S:5/4 or a CLR instruction with S:5. Reserved for minor errors that revert to major errors at the end of the scan. Memory Module Boot Bit When this bit is set by the processor, it indicates that a memory module program	•	•	•	•	•

		on entry into the REM Run mode to determine if the memory module content has been transferred. Bit S:1/15 will be set to indicate REM Run mode entry. This information is useful when you have an application that contains retentive data and a memory module that has only bit S:1/10 set (Load Memory Module on Memory error). Use this bit to indicate that retentive data has been lost. This bit is also helpful when using bits S:1/11 (Load Memory Module Always) or S:1/12 (Load Memory Module Always and Run) to distinguish a power up REM Run mode entry from a REM Program (or REM	•	•	•	•
	Status	Test) mode to REM run mode entry. Memory Module Password Mismatch Bit This bit is set on REM Run mode entry, whenever loading from the memory module is specified (word 1, bits 11 or 12) and the processor user program is password protected, and the memory module program does not match that password. Use this bit to inform your application program that an autoloading memory module is installed but did not load due to password mismatch.	•	•	•	•
S:5/10	Status	STI (Selectable Timed Interrupt) Overflow Bit This bit is set whenever the STI timer expires while the STI routine is either executing or disabled and the pending bit is already set.		•	•	•
S:5/11	Status	Battery Low Bit This bit is set whenever the Batter Low LED is on. The bit is cleared when the Batter Low LED is off.		•	•	•
S:5/12	Status	Discrete Input Interrupt Overflow Bit This bit is set whenever the DII interrupt occurs while still executing the DII subroutine or whenever the DII interrupt occurs while pending or disabled.		•	•	•
S:5/13	Dynamic Config	Unsuccessful Operating System Load Was Attempted This bit is set whenever an operating system memory module load is attempted and is unsuccessful. Unsuccessful loads can occur when either the protection jumper is		•	•	•

		I,	l I	1	
		in the protect position or is missing, or if			
		the operating system memory module is			
		incompatible with the SLC 5/03, SLC			
		5/04, or SLC 5/05 processors' hardware			
		platform. Examine the state of this bit with			
		your user program to diagnose the			
		condition			
S:5/14	Status	Channel 0 Modem Lost			
0.0, = .		This bit indicates the status of the modem			
		connected to Channel 0 (RS232 serial port).			
		The state of the bit is determined by:			
		the protocol Channel 0 is configured			
		for,			
		the Control Line selected, and			
		the states of DCD (Data Carrier DCD (Data Carrier)			
		Detect) and DSR (Data Set Ready).			
		If the bit is set, then the modem is not			
		properly connected to Channel 0 or it is in a			
		state where unreliable communication			
		exchanges may take place via Channel 0.			
		The following conditions apply:			
		 If Channel o is disabled or configured 			
		for DH485, the bit is always cleared.			
		 If Channel 0 is configured for one of 			
		the DF-1 protocols in System Mode or			
		Generic ASCII in User Mode, then the			
		Control Line selection determines			
		how DCD and DSR affect the modem			
		status:			
		o If Control Line=NO			
		HANDSHAKING: The bit is always			
		set.			
		HALF-DUPLEX WITHOUR			
		CONTINUOUS CARRIER: The bit			
		is set if DSR goes inactive and			
		cleared when DSR goes active.			
		(DCD has no effect on modem			
		status in this case).			
		O If Control Line=HALF-DUPLEX			
		WITH CONTINUOUS CARRIER:			
		The bit is set is either DSR goes			
	1	inactive or DCD remain inactive			
		for more than 10 seconds. This			
	1	bit is cleared when both DSR and			
		DCD go active.			
S:5/15	Status	ASCII String Manipulation Error			
		This bit applies to SLC5/03 (OS301and			
		higher), SLC 5/04, and SLC 5/05 processors.			
	<u> </u>	111611617, 316 3/04, and 316 3/03 processors.	<u> </u>	1	

	1	This bin is sain at 1 and 1		l			
		This bit is set to 1 when an attempt is made			•	•	•
		to process a string using an ASCII					
		instruction that exceeds 82 characters in					
S:6	Status	length. Major Error Fault Code					
3.0	Status	A hexadecimal code is entered in this word					
		by the processor when a major error is					
		declared. Refer to S:1/13. The code defines					
		the type of fault, as indicated on the					
		following pages. This word is not cleared by					
		the processor. Error codes are presented,	_			_	_
		stored and displayed in a hexadecimal	•	•	•	•	•
		format. Refer to appendix G for more					
		information on the hexadecimal numbering					
		system.					
		If you enter a fault code as a parameter in					
		an instruction in your ladder program, you					
		must convert the code to decimal. For					
		example, if you program an EQU					
		instruction to go true when the error 0016					
		occurs, enter S:6 as source A and 22, the					
		EQU -					
		Source A S:6					
		Source B 22					
		304208 3					
		decimal equivalent of 0016H, as source					
		B:					
		Application Example: You can declare your					
		own application specific major fault by					
		writing a unique value to S:6 and then					
		setting bit S:1/13.					
		SLC 5/02 processor users: Interrogate the					
		value of S:6 in your fault routine to					
		determine the type of fault that occured. If					
		your program was saved with the					
		test single step enabled, you can also					
		interrogate S:20 and S:21 to pinpoint					
		the exact rung that was executing when the					
		fault occurred. Fault Classifications: Faults					
		are classified as Non-User, Non-					
		Recoverable, and Recoverable.					
		Non-User Fault					
		The fault routine does not execute.					
		Non-Recoverable User Fault					
		The fault routine executes for 1 pass. (You					
		may initiate a MSG instruction					
		to another node to identify the fault					

condition of the processor). Recoverable User Fault The fault routine may clear the fault by clearing bit S:1/13. Error code descriptions and classifications are listed on pages through. Categories are: o powerup errors o going-to-run errors o runtime errors o user program instruction errors o II/O errors See chapter 15 of this manual for fault cause and recovery information.			

SAFETY BULLETIN

This notice is issued to advise you that some previously accepted shop practices may not be keeping up with changing Federal and State Safety and Health Standards. Your current shop practices may not emphasize the need for proper precautions to insure safe operation and use of machines, tools, automatic loaders and allied equipment and/or warn against the use of certain solvents or other cleaning substances that are now considered unsafe or prohibited by law. Since many shop practices may not reflect current safety practice and procedures, particularly with regard to the safe operation of equipment, it is important that you review your practices to ensure compliance with Federal and State Safety and Health Standards.

IMPORTANT

The operation of any machine or power-operated device can be extremely hazardous unless proper safety precautions are strictly observed. Observe the following safety precautions:

ALWAYS:

- ✓ Be sure proper guarding is in place for all pinch, catch, shear, crush, and nip points.
- ✓ Be sure that all personnel are clear of the equipment before starting it.
- ✓ Be sure the equipment is properly grounded.
- ✓ Turn the main electrical panel off and lock it out in accordance with published lockout/tagout procedures prior to making adjustments, repairs, and maintenance.
- ✓ Wear appropriate protective equipment such as safety glasses, safety shoes, hearing protection, and hard hats.
- ✓ Keep chemical and flammable material away from electrical or operating equipment.
- ✓ Maintain a safe work area that is free from slipping and tripping hazards.
- ✓ Be sure appropriate safety devices are used when providing maintenance and repairs to all equipment.



NEVER:

- ✓ Exceed the rated capacity of a machine or tool.
- ✓ Modify machinery in any way without prior written approval of the Besser Engineering Department.
- ✓ Operate equipment unless proper maintenance has been regularly performed.
- ✓ Operate any equipment if unusual or excessive noise or vibration occurs.
- ✓ Operate any equipment while any part of the body is in the proximity of potentially hazardous areas.
- ✓ Use any toxic flammable substance as a solvent cleaner.
- ✓ Allow the operation or repair of equipment by untrained personnel.
- ✓ Climb or stand on equipment when it is in operation.

It is important that you review Federal and State Safety and Health Standards on a continual basis. All shop supervisors, maintenance personnel, machine operators, tool operators, and any other person involved in the setup, operation, maintenance, repair or adjustment of Besserbuilt equipment should read and understand this bulletin and Federal and State Safety and Health Standards on which this bulletin is based.

